REMARKS/ARGUMENTS

Request for Continued Examination:

The applicant respectfully requests continued examination of the above-indicated application as per 37 CFR 1.114.

1. Introduction

This is a full and timely response to the Office action of August 16, 2007. Claims 1, 10-12, 18, and 40 are currently amended, and new claims 43-47 are introduced.

10 Reconsideration of all claims in the present application is respectfully requested.

2. Background

Claims 1, 4-7, 9-15, 17-25, and 27-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaku et al., US Patent 6,414,932, in view of Kato et al., US Patent 6,775,217 in view of Han, US Patent 7,102,976. Claims 8 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaku et al. in view of Kato et al. in view of Han, and further in view of Chung et al., US Patent 4,873,680.

3. Response

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- Independent claims 1 and 40 have been amended to overcome these rejections.

 Claims 15, 17, 19-39, and 41-42 have been cancelled. All amendments are made without prejudice or disclaimer to subject-matter and the Applicant reserves the rights to reintroduce any deleted matter in this, or any subsequent divisional application.
- Claim I now recites that a clock generator generates distinct first and second clock signals. Claim I also states that a delay adjustment state machine generates a rough delay parameter and a fine delay parameter according to the selected set of write strategy parameters, and delays the RLL modulation waveform according to the second clock signal and the set of write strategy parameters so as to generate a second delay signal.

In contrast, the cited prior art fails to disclose the delay adjustment state machine "delaying the RLL modulation waveform according to the second clock signal and the set of write strategy parameters so as to generate a second delay signal".

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As evidenced by the Office action dated January 05, 2007, the Examiner's position is that:

- The delay adjustment state machine is part of element 114 (Fig. 2 of Kaku).
- b) The second clock signal refers to SCLK and is transferred to the delay adjustment state machine through the "internal data bus" shown in Fig. 2 of Kaku.
- c) The delay adjustment state machine delays the RLL modulation waveform according to the second clock and the set of write strategy parameters (Column 2, lines 38-40 of Kaku).

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However,

- a) Kaku fails to disclose a delay adjustment state machine.
- b) Kaku fails to disclose that the "internal data bus" transfers the clock signal SCLK into the write strategy control unit 104. As one can see, Kaku only illustrates the internal data bus in Fig. 2, but fails to provide more detailed descriptions, such as, what the structure of the bus is and how the bus operates. Therefore, one of skilled in the art cannot realize how the "SCLK is transferred to the delay adjustment state machine through the internal data bus".

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c) Further, Kaku fails to disclose the delay adjustment state machine delays the RLL modulation waveform according to the second clock and the set of write strategy parameters. The cited paragraph (col. 2, lines 38-40) only disclose "For this the delay circuit is provided for the purpose of bring the NRZ modulation signal from the modulation circuit into line with the reflection light in timing thereof". From this one skilled in the art cannot

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realize how the teaching of this paragraph has a relationship with "the delay adjustment state machine", and further has the relationship with the delay adjustment state machine "delaying the RLL modulation waveform according to the second clock and the set of write strategy parameters".

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In summary, Kaku fails to disclose the delay adjustment state machine "delaying the RLL modulation waveform according to the second clock signal and the set of write strategy parameters so as to generate a second delay signal", as is recited in the currently amended claim 1.

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Claim 40 recites the limitation of "wherein the fine delay chain is not connected to and does not utilize a clock signal for delaying the first delay signal to generate the write signal." In a telephone interview between Patent Agent Scott Margo (Reg. No. 56,277) representing the applicant and Examiner Parul Gupta, the Examiner stated that Kato teaches this limitation of claim 40 by teaching in column 5, lines 29-40 generating delay parameters without the use of a clock. Mr. Margo then pointed out that Kato's delay chain that the Examiner was relying upon to reject the claimed fine delay chain was the ring oscillator 500 shown in Fig.5 of Kato, and that from looking at Figures 3 and 5, Kato teaches that the multi-phase clock synthesizer 320 and the ring oscillator 500 are both connected to a reference clock. The Examiner said that this appeared to be correct, but that it was not clear from the instant application that the fine delay chain of the instant application did not also rely upon a clock for delaying the first delay signal.

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However, the key point of this limitation of claim 40 is the language "not connected to and does not utilize a clock signal for delaying the first delay signal". Claim 40 does not claim "not connected to and does not utilize a clock signal for delaying the second delay signal or the RLL modulation waveform". Simply speaking, the fine delay chain is utilized to process "the first delay signal". Before the first delay signal is processed by the fine delay chain, the first delay signal might be

generated associating with a clock signal. However, when the fine delay chain delays the first delay signal, it is not needed to connect and utilize a clock signal. Thus, one skilled in the art would not interpret that the fine delay chain, as shown in Figs. 2 and 3 of the instant application, delays the first delay signal by utilizing a clock signal. For these reasons, the applicant submits that the cited prior art fails to teach all of the limitations of claim 40.

Furthermore, as claims 4-14 and 18 are dependent on claim 1, claims 4-14 and 18 should be allowed if claim 1 is allowed. Reconsideration of claims 1, 4-14, 18, and 40 is therefore respectfully requested.

4. Introduction to new claims 43-47

New dependent claims 43-47 are added and are drafted to be dependent on claim 1. New claims 43 and 44 are supported by the original claim 16 along with the specification and drawings of the instant application as filed. New claim 45 is a substantial duplicate of the distinguishing limitation of claim 40, found at the end of claim 40. Claim 46 is a duplicate of claim 36, now cancelled. Claim 47 is supported in claim 19, now cancelled. No new matter has been added through any of the new dependent claims 43-47, and consideration of claims 43-47 is respectfully requested.

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Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

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Appl. No. 10/604,862 Reply to Office action of August 16, 2007 JAN 1 4 2008

Sincerely yours,

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)